

# Supplemental material: Thermal Conductance of a Single Electron Transistor

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In this supplemental material part, we discuss details of the sample fabrication process, estimation of the SET and NIS probe parameters from independent electrical measurements, as well as the thermal balance. We add complementary experimental data that supports the analysis made in the main paper.

## SAMPLE FABRICATION

The SET samples are fabricated using a process closely related to the one described in Ref. S1, relying on two rounds of electron beam lithography (EBL) and subsequent metal depositions. The substrate is a p-doped (resistivity  $1 - 30 \Omega\text{cm}$ ), single-side polished 4" Si (100) wafer with 300 nm thermal oxide grown on both sides.

In the first lithography round, a large-area continuous ground plane electrode is patterned and subsequently metallized in an electron beam evaporator as a stack of Ti (2 nm) / Au (30 nm) / Ti (2 nm). After liftoff, the full wafer is coated with an approximately 50 nm thick insulating layer of  $\text{Al}_2\text{O}_3$ , grown by atomic layer deposition (ALD). The ground plane electrode starts approximately 20  $\mu\text{m}$  away from the SET junctions and the NIS probes [not visible in Fig. 1 (b)]. Overlap of the SET and NIS probe leads, defined in the second lithography step, with this ground plane electrode forms an efficient on-chip filter against residual microwave-frequency noise [S2]. The two thin Ti layers help with adhesion to the  $\text{SiO}_2$  substrate and the initial growth of the  $\text{Al}_2\text{O}_3$  dielectric.

Following the ALD growth, a suspended Ge-based hard mask is prepared for the main EBL step where all the structures shown in Fig. 1 (b) are defined. The total thickness of the mask is typically 400 – 500 nm, whereas the e-beam deposited Ge layer is only 22 nm thick, making it possible to optimize the lithography and development steps for reliable formation of the small tunnel junctions. The sacrificial layer under Ge is formed by a spin-coated layer of P(MMA-MAA) copolymer. Immediately after the multi-step dry development process by reactive ion etching (RIE) in  $\text{CF}_4$  and  $\text{O}_2$  plasmas,

the sample is loaded into an evaporator equipped with a tiltable sample holder. This allows fabricating both the normal-metal SET and the NIS probes using the same mask and in a single vacuum cycle. The SET is realized using an adaptation of the technique introduced in Ref. S4 as discussed in the following.

First, a 30 nm (45 nm) thick film of Cu is deposited for sample A (B) with the sample holder set to normal incidence with respect to the evaporation source. As indicated in Fig. 1a, this initial Cu layer forms the SET drain lead as well as the main part of the source electrode. This is immediately followed by the evaporation of a 20 nm layer of Al. For this deposition, the sample holder is now tilted to an angle close to  $38^\circ$ , resulting in an effectively close to 15 nm thick, downwards [in the orientation of Figs. 1(b) and S1] shifted Al copy of the mask pattern. The Al layer forms the two, sub-200 nm long dots, connected to the source and drain Cu regions with transparent metal-to-metal contacts. As observed in Ref. S4, the Al pieces, with length comparable to the superconducting coherence length, are driven normal due to strong inverse proximity effect from the Cu electrodes. As evident from Fig. 1 (b), the same Al deposition also forms the S electrodes of the NIS thermometer and cooler/heater [colored light blue in Figs. 1 (a) and (c)]. To form the  $\text{AlO}_x$  tunnel barriers for the SET and NIS probe tunnel junctions, the Al layer is subjected to *in-situ* static oxidation immediately after the deposition is completed. This is accomplished by letting typically 1 – 2 mbar of oxygen into the deposition chamber for the duration of 60 – 90 s.

To complete the fabrication, a second 30 nm layer of Cu is evaporated with the sample now tilted  $25^\circ$  in the opposite direction compared to the preceding Al deposition. This upwards-shifted copy of the mask pattern forms the SET island [yellow in Figs. 1 (a)–(b)] as well as the N electrode of the NIS probes. As a result of the three-angle evaporation through the same mask, three projections of the complete mask pattern will be formed on the substrate. The irrelevant, partially overlapping shadow copies of the various structures, evident in Figs.

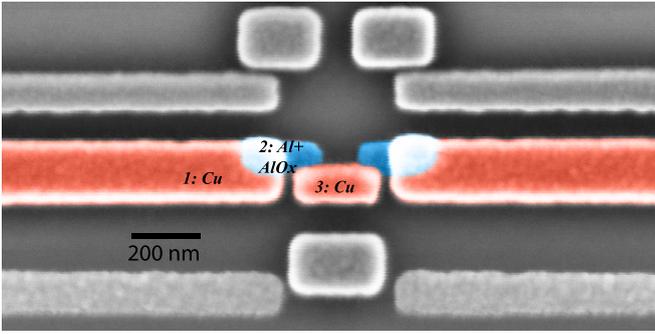


FIG. S1. False-color scanning electron micrograph of a normal-metallic SET realized with shadow-evaporated Al-proximity junctions. The coloring indicates the materials, and the labels show the order in which the three films are deposited.

1 (b) and (c), are shown uncolored in gray.

### SAMPLE DESIGN

The length of the narrow and fully superconducting source electrode, i.e., the region where it is not overlapped by the Cu structures and is therefore completely unaffected by the inverse proximity effect, is approximately  $3 \mu\text{m}$ . At electronic temperatures up to about 250 mK, this is sufficient for very good thermal isolation of the SET source close to the tunnel junctions [S5].

The source is made of three Cu elements in series, made of two distinct layers, see Fig. 1(a). The Cu–Cu contacts between these elements have low electrical and thermal resistance, as the first Cu film is not significantly oxidized during the formation of the *in-situ*  $\text{AlO}_x$  tunnel barriers. Therefore, no thermal gradient will develop between the three Cu islands forming the normal-conducting part of the SET source electrode.

We note that in the present work the deposition order for the SET junctions differs from Ref. S4. Instead of depositing the Al first, followed immediately by Cu in direct contact, and only then oxidizing the Al, we now start with Cu as detailed above. This reversed order for forming the transparent Al-Cu contact allows better experimental control over the tunnel junction transparencies.

Let us estimate the electron-phonon coupling power in the SET island at the maximum-phonon cooling point in main paper Fig. 2 data. The electron temperature  $T_e$  varies between 92 and 95 mK for a bath temperature of 152 mK. If we estimate that the island electron temperature is the mean between the drain (bath) temperature and the source temperature, we find a value of about 123 mK. With the island volume of  $5.8 \cdot 10^{-4} \mu\text{m}^3$ , we obtain a power of 88 aW. This can be compared to the power through the SET of 1.43 fW at  $n_g = 1/2$ . The electron-

phonon power is thus only 5.9 % of the power through the SET. It can thus be safely neglected.

### SET CHARACTERIZATION

To model the thermal transport properties of the SET, we need to estimate the charging energy  $E_C$  and the tunneling resistance  $R_T$ . Assuming symmetric junctions with identical resistances  $R_T/2$ , a straightforward and reliable way to obtain them is to make a fit to the measured minimum and maximum current  $I_{\text{SET}}$  at each bias voltage  $V_{\text{SET}}$ . An example of such calculated envelope curves at  $T_b = 72 \text{ mK}$ , corresponding to  $I_{\text{SET}}$  at  $n_g = 0$  and at  $n_g = 1/2$ , is included in Fig. S2 for sample B. From this procedure, performed at several bath temperatures  $T_b$ , we estimate  $E_C = 155 \mu\text{eV}$  and  $R_T = 82 \text{ k}\Omega$  for sample A,  $E_C = 100 \mu\text{eV}$  and  $R_T = 26 \text{ k}\Omega$  for sample B. For an improved estimate of  $E_C$ , we include self-heating at finite currents  $I_{\text{SET}}$  and solve the SET source temperature consistently from the thermal balance equation.

At the charge degeneracy point  $n_g = 0.5$ , the current-voltage characteristic is linear. This confirms that the inverse proximity in the SET leads is effective and that they are well in the normal state.

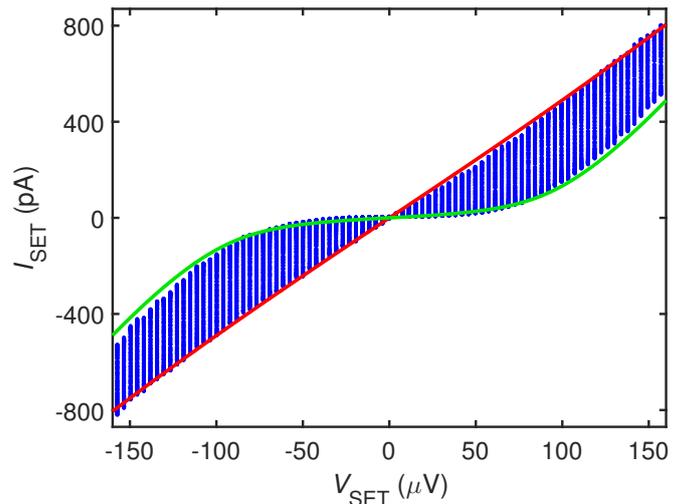


FIG. S2. Sample B SET current plotted for different values of the induced charge  $n_g$  as a function of  $V_{\text{SET}}$ , together with envelope curves calculated at  $n_g = 0$  (green) and at  $n_g = 1/2$  (red).

### NIS THERMOMETER AND COOLER CHARACTERIZATION

Here we show how the main parameters that describe the NIS junction cooler current and its cooling power  $\dot{Q}_{\text{NIS}}$  were estimated. These include the normal state

tunnel resistance  $R_{T,NIS}$ , low-temperature superconducting energy gap  $\Delta$ , and the dimensionless Dynes broadening parameter  $\gamma$ . To this end, we fit the measured NIS junction IV characteristic using [S3]:

$$I_{NIS} = \frac{1}{2eR_{T,NIS}} \int_{-\infty}^{\infty} dE n_S(E) [f_{source}(E - eV_{NIS}) - f_{source}(E + eV_{NIS})], \quad (S1)$$

showing explicitly that  $I_{NIS}(V_{NIS}) = -I_{NIS}(-V_{NIS})$ , and that  $I_{NIS}$  depends directly only on the electronic temperature  $T_e$  of the SET source electrode. We include the  $V_{NIS}$ -dependence of  $T_e$  via a basic thermal balance.

The low-temperature IV characteristic of the NIS cooler junction of sample B is included in Fig. S3, both on linear and logarithmic scale, together with the calculated  $I_{NIS}$ . For this sample we obtain  $R_{T,NIS} = 13.2 \text{ k}\Omega$ ,  $\Delta = 208 \text{ }\mu\text{eV}$ , and  $\gamma = 8 \times 10^{-4}$ . When compared to effects caused by the overheating of the superconducting electrode, the exact value of  $\gamma$  or other subgap features of the I-V curve do not play a significant role in modeling the cooling power of the NIS junction at voltages  $V_{NIS}$  close to  $\Delta/e$ .

### HEAT BALANCE

As a simplification for SETs with high normal state resistance, we assume that  $\dot{Q}_{SET}$  fulfills the Wiedemann-Franz law at  $n_g = 0.5$  (“gate open”). We then model the actual cooling power of the NIS junction by using an elevated  $T_S > T_b$ , caused by the injection of non-equilibrium quasiparticles at  $eV_{cool} \approx \Delta$ . At  $T_b \approx 150 \text{ mK}$ , the superconductor temperature shows values  $T_S \approx (250 - 450) \text{ mK}$ , cf. Fig. S4. The order of magnitude of the  $T_S$  appears realistic when compared to experiments in similar structures [S9]. Such a consistent behavior is obtained for bath temperatures up to 300 mK where thermal leakage through the superconducting lead of the source starts to contribute significantly.

Once the elevated  $T_S$  has been extracted in the above manner, we can use it as well as the *measured*  $T_e$ , to extract  $\dot{Q}_{SET}$  from the heat balance. Notably, this procedure is independent of the model for the SET heat flows – it rests only on the assumption that  $\dot{Q}_{SET}(n_g = 0.5)$  fulfills the Wiedemann-Franz law.

In the linear regime, the thermal conductance is proportional to temperature:  $\kappa = \sigma_0 L T$ . If one considers a temperature drop between  $T_e$  and  $T_b$ , one obtains:

$$\begin{aligned} P &= \int_{T_e}^{T_b} \sigma_0 L dT = \frac{\sigma_0 L}{2} (T_b^2 - T_e^2) = \sigma_0 L \frac{T_b + T_e}{2} (T_b - T_e) \\ &= \sigma_0 L T_m (T_b - T_e) \end{aligned} \quad (S2)$$

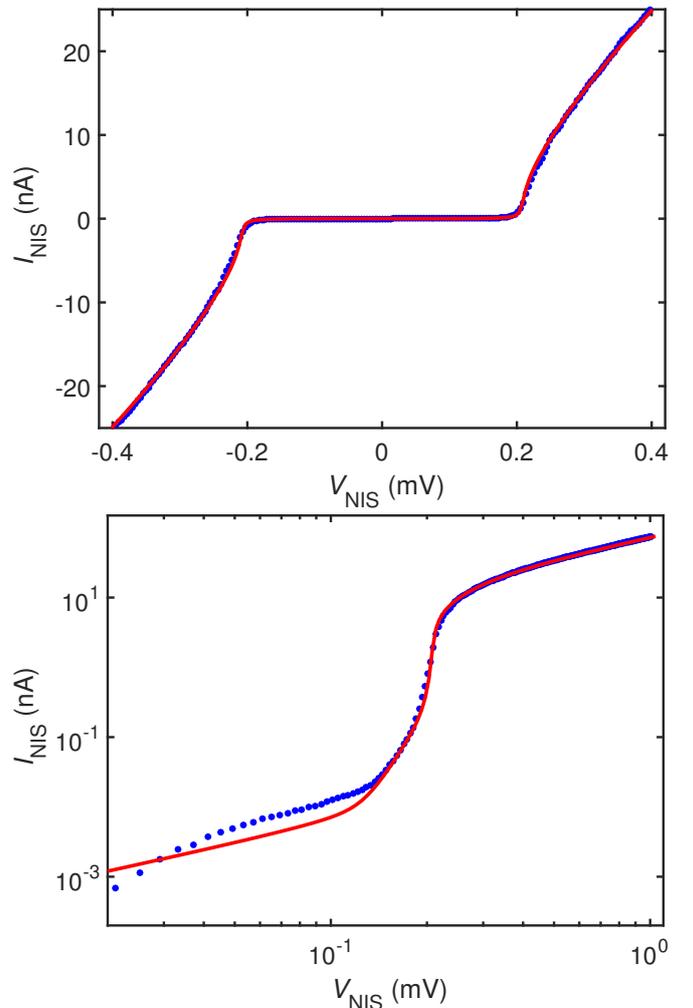


FIG. S3. Current–voltage characteristic of one NIS junction of sample B on (top) linear and (bottom) logarithmic scale. Fits are shown as full red lines.

where  $T_m = (T_b + T_e)/2$ . Considering the Wiedemann-Franz value for the thermal conductance at the mean temperature  $T_m$  then enables one to obtain a linear behavior.

### ADDITIONAL EXPERIMENTAL MATERIAL

The analysis displayed in Fig. 3 of the main paper can be performed also in the heating regime, see Fig. S5. In that case, the temperature difference is significant. It is then particularly important to use, in the calculation of the Lorenz factor, the temperature that is the mean between the cold side (the bath temperature) and the hot side (the electron temperature). Fig. S5 shows a similar behavior to the one observed in main paper Fig. 3.

Figure S6 displays the gate dependence of both the electron-phonon power and the power flowing through the SET for sample B at the maximum cooling point.

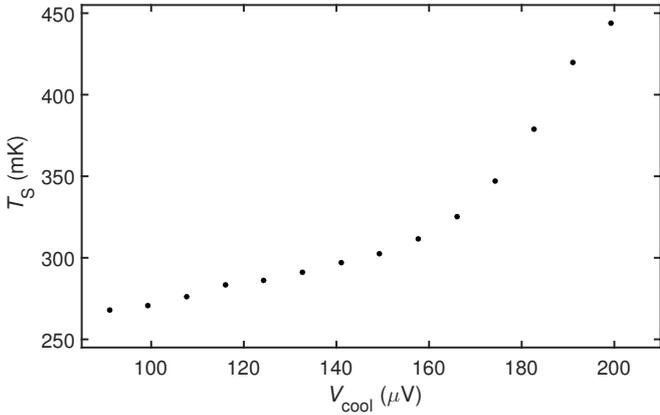


FIG. S4. Calculated value of the NIS cooler superconductor temperature  $T_S$  for sample B, used in the fit of Fig. 2 (main paper) data.

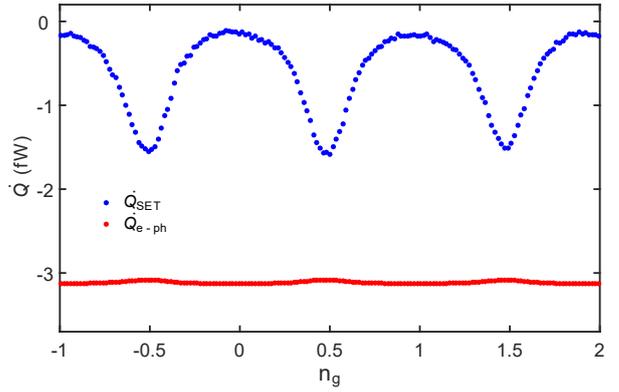


FIG. S6. Dependence of the electron-phonon coupling power  $\dot{Q}_{e-ph}$  and the power flow through the SET  $\dot{Q}_{SET}$ , on the gate potential, related to the data of Fig. 2 in the main text.

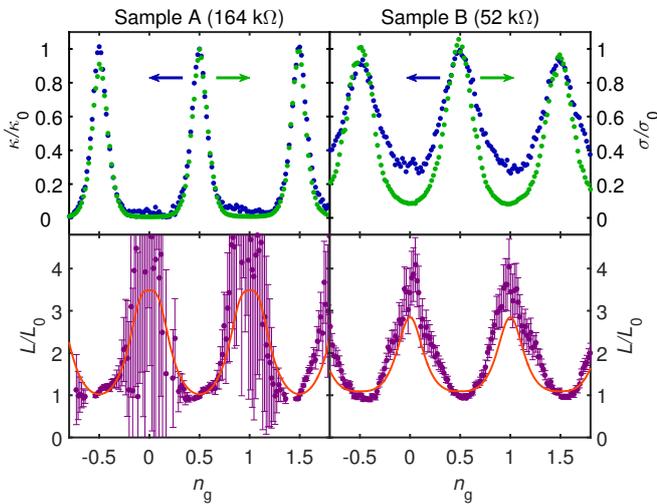


FIG. S5. Top: Thermal and electrical conductances of the SET for sample A (left) and sample B (right) at a bath temperature of 132 mK (sample A) and 152 mK (sample B). The thermal flow through the SET was calculated assuming that the Wiedemann-Franz law is fulfilled at gate-open state. The charge transport measurement was done at a bias of 22.4  $\mu\text{V}$  (sample A) and 19.2  $\mu\text{V}$  (sample B). The heat transport data was acquired by heating the source electronic bath by 60 mK (sample A) and 52 mK (sample B) above the bath temperature. Bottom: Lorenz ratio defined as  $L/L_0$  where  $L = \kappa/(\sigma T_m)$  for sample A (left) and sample B (right). The red line is the theoretical prediction.

It is observed that the power flow through the SET can represent up to 50% of the total power flow at 150 mK.

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